Notice of Allowability	Application No.	Applicant(s)	
	09/587,529	KOJIMA ET AL.	
	Examiner	Art Unit	
	Quang N. Nguyen	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed on 03/16/2006*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JASON CARDONE
SUPERVISORY PATENT EXAMINER

Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this Examiner's Amendment was given in a telephone interview with the Applicant's Representative, Mr. Dexter Chang (Reg. No. 44,071), on May 11th, 2006.

3. Please amend claims 1, 4 and 8 as below:

1. (Currently amended) A packet data processing apparatus for processing a packet received from a network by a processor, comprising:

a packet data access part, which has a plurality of registers **and a plurality of selectors** arranged in series, shifting the received packet through the plurality of registers toward an outlet in synchronization with a clock,

wherein:

the processor processes the received packet while the received packet is being-shifted through the plurality of registers, independently of an instruction order for processing the received packet;

the processor and the packet data access part are directly connected by a read data line and a write data line;

the processor reads out or writes data from or to the packet data access part by synchronizing the cycle time of the processor by the read data line and the write data line; and

each of the plurality of registers of the packet data access part is connected to a neighbor register via **one of the plurality of selectors** [~~a selector~~] which selects write data from between the processor **via the write data line** and the neighbor register, so as to enable the processor to process the received packet, instead of fully shifting the received packet through the entire series of registers.

4. (Currently amended) The packet data processing apparatus as claimed in claim 1, wherein said processor processes the received packet being shifted[[r]] by said packet data access part in accordance with a set of instructions.

8. (Currently amended) A packet relay apparatus for forwarding a packet received from a network, comprising:

a plurality of processors being connected in series in that the packet sequentially passes through the plurality of processors, each processor comprising:

a packet data access part, which has a plurality of registers **and a plurality of selectors** arranged in series, shifting the received packet through the plurality of registers toward an outlet in synchronization with a clock,

wherein:

the processor processes the received packet while the received packet is being-shifted through the plurality of registers, independently of an instruction order for processing the received packet;

the processor and the packet data access part are directly connected by a read data line and a write data line;

the processor reads out or writes data from or to the packet data access part by synchronizing the cycle time of the processor by the read data line and the write data line; and

each of the plurality of registers of the packet data access part is connected to a neighbor register via **one of the plurality of selectors** [~~a selector~~] which selects write data from between the processor **via the write data line** and the neighbor register, so as to enable the processor to process the received packet, instead of fully shifting the received packet through the entire series of registers.

4. Claims 1-12 are allowed.

5. The following is an examiner's statement of reasons for allowance:

In interpreting the claims, in light of the specification and the applicant's arguments filed on 03/16/2006, the Examiner finds the claimed invention to be patentably distinct from the prior art of record.

McMurray et al. (US 4,145,686), teach a data compressor with a plurality of serially connected shift registers within memory 28, as illustrated in Fig. 2, compressing digital signals received from a data lift 22 for transfer to a storage device, wherein a sequencer 41 provides a clock pulse which is synchronized with the pulse to shift the data through the memory 28 at the same rate as it is generated within the data lift 22 **(McMurray, Fig. 2 and C4: L11-23)**.

Toda (US 5,076,133) teaches a musical tone signal apparatus with two sets of registers to be connected in serial, each consisting of the selector and shift register, as illustrated in Fig. 5, wherein the selector performs the selecting operation thereof in response to a data change write signal DC. When the data change write signal DC is changed from "0" to "1", the shift register 220 inputs the external waveform data. At a timing when a control signal TS supplied to the selector 221 is changed from "0" to "1", contents of data stored in the shift register 222 is renewed by new external waveform data **(Toda, Figs 1 and 5, C6: L33-44)**.

Klim et al. (US 5,732,233), teaches a data processing apparatus that has a number of data processors connected in a series by data lines *(Pa, Pb, Pc and Pd as*

illustrated in Fig. 3) so that data signals are processed in a preceding processor and communicated to a succeeding processor in the series **(Klim, Fig. 3 and C4: L34-37)**.

However, the prior art of records fail to teach or suggest individually or in combination that a packet data processing apparatus for processing a packet received from a network by a processor, comprising: **a packet data access part, which has a plurality of registers and a plurality of selectors arranged in series**, shifting the received packet through the plurality of registers toward an outlet in synchronization with a clock, wherein: the processor processes the received packet while the received packet is being-shifted through the plurality of registers, independently of an instruction order for processing the received packet; the processor and the packet data access part are directly connected by a read data line and a write data line; the processor reads out or writes data from or to the packet data access part by synchronizing the cycle time of the processor by the read data line and the write data line; and **each of the plurality of registers of the packet data access part is connected to a neighbor register via one of the plurality of selectors which selects write data from between the processor via the write data line and the neighbor register, so as to enable the processor to process the received packet, instead of fully shifting the received packet through the entire series of registers** as set forth in claims 1 and 8. Claims 1-12 are allowed because of the combination of other limitations and the limitations listed above.

The examiner finds the Applicant's arguments on pages 7-9 of the Remarks filed on 03/16/2006 to be persuasive. The Applicant argued in substance that the combination of prior art of records fail to disclose the features of the invention including *each of the plurality of registers of the packet data access part is connected to a neighbor register via one of the plurality of selectors which selects write data from between the processor via the write data line and the neighbor register, so as to enable the processor to process the received packet, instead of fully shifting the received packet through the entire series of registers*, as claimed in the invention to provide the mechanism for directly reading out and writing the packet data, transmitting data independent of the instruction order and to eliminate the disadvantage related to the conventional reading process and writing process, i.e., to provide the high speed packet process with high flexibility based on the instruction order **(see Specification, page 13, line 22 – page 15, line 5)**.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should clearly labeled "Comments on Examiner's Amendment".

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Nguyen whose telephone number is (571) 272-3886.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's SPE, Rupal Dharia, can be reached at (571) 272-3880. The fax phone number for the organization is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JASON CARDONE
SUPERVISORY PATENT EXAMINER